Exhibit D

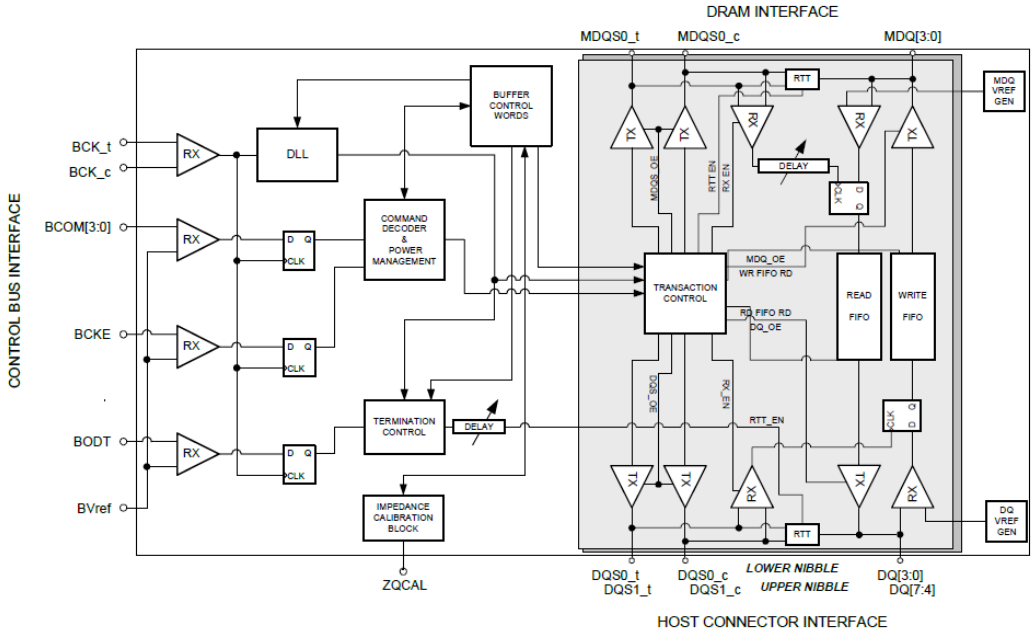
[redacted]

Exhibit D – Infringement of U.S. Patent No. 10,268,608

Netlist notes that these preliminary infringement contentions are based on publicly available information. Netlist expects that information to be revealed in future discovery may result in identification of additional instances of Samsung's infringement, and may also enable identification of additional claims infringed by Samsung. The claims asserted, and the theories set forth herein are based on Netlist's present understanding of the Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, these contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions. On information and belief, the examples are representative of the Accused LRDIMM products in material aspects.

The Accused Instrumentalities include Samsung's Double Data Rate 4 ("DDR4") load reduced dual in-line memory modules ("LRDIMMs"). By way of non-limiting example, the accused DDR4 LRDIMM products include, without limitation, Samsung products having the following part numbers: M386A4K40BB0-CRC, M386A8K40BM1-CRC, M386A8K40BM2-CTD, M386A8K40BMB-CRC, M386A8K40CM2-CRC, M386A8K40CM2-CTD, M386A8K40CM2-CVF, M386A8K40DM2-CTD, M386A8K40DM2-CVF, M386A8K40DM2-CWE, M386AAG40AM3-CWE, M386AAG40MM2-CVF, M386AAG40MMB-CVF, M386AAK40B40-CUC, M386AAK40B40-CWD, M386ABG40M50-CYF, M386A8K40BMB-CPB, M386A8K40BM1-CPB, M386ABG40M51-CAE, and M386ABG40M5B-CYF. The Accused Instrumentalities also include any other Samsung DDR4 LRDIMM products made, sold, offered for sale, imported and/or used by Samsung that are JEDEC-standard compliant memory modules. Examples of Samsung's DDR4 LRDIMM products, reproduced below, can be found via Samsung's module-selector web page. See Module: Memory Modules For Extensive Use, Samsung, available at https://www.samsung.com/semiconductor/dram/module.

Samsung also infringes through acts of inducement and contributory infringement.

Claim 1	Evidence of Use
data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.	signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. As shown below, the data paths through the DDR4 data buffer, i.e., between the individual DRAMs connected to the DRAM Interface and the data/strobe signal lines of the Host Connector Interface, include tristate buffers and a delay circuit. The tristate buffers are controlled by processing circuitry, which may include but not be limited to the depicted transaction control module, DLL, command decoder & power management module, termination control module, buffer control words module, etc. **4.61 Logic Diagram**  **Figure 15 — Logic Diagram** *See, e.g.,* JEDEC 82-32A Standard, p. 95. For example, the DDR4 data buffers support certain modes, *e.g.*, the DRAM-to-DB Read Delay (MRD) Training Mode. The MDQS delay adjustment are performed in the DDR4 data buffer for each rank, *e.g.*, of four ranks [3:0] using two sets of registers F[3:0]BC4x for the lower nibble and F[3:0]BC5x for the upper